9. The arrangement of claim 8 wherein the integrator is of an n-th order.

10. The arrangement of claim 8 wherein the delay stage is configured to adjust a sequence of digital input values.

11. The arrangement of claim 8 wherein the decimator is configured to convert the input value into a sequence of digital output values.

12. The arrangement of claim 8 wherein the decimator is configured to use a non-integral factor defined by $M + \alpha$, where M is a positive integer and α is greater than zero and less than one.

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13. The arrangement of claim 9 wherein the delay stage is defined by m times k, where m is a positive integer and k is the delay factor.

14. The arrangement of claim 8 wherein the interpolation arrangement interpolates between a plurality of intermediate output values having k/f intervals, wherein k is a delay factor determined by the delay stage and f is a sampling rate.

15. The arrangement of claim 8 wherein the interpolation arrangement includes a switching device connected to the differentiator.

16. The arrangement of claim 15 wherein the interpolation arrangement further includes an amplifier arrangement connected to the switching device.

17. The arrangement of claim 16 wherein the switching device is configured to receive the input value from the differentiator and generate the decimated output value sent to the amplifier arrangement.

18. The arrangement of claim 15 wherein the interpolation arrangement further includes an adder for combining the decimated output value of the amplifier arrangement.

19. The arrangement of claim 16 wherein the amplifier arrangement includes a first amplifier and a second amplifier, the first amplifier having a gain factor of α and the second amplifier having a gain factor of $1-\alpha$, wherein α is greater than zero and less than one.

20. The arrangement of claim 8 wherein the interpolation arrangement is configured to generate a linear interpolation.

21. The arrangement of claim 15 further comprising a control device for switching the switching device in accordance with the intermediate output value received by the interpolation arrangement.

22. The arrangement of claim 21 wherein the control device is configured to determine the delay factor of the delay stage by adjustably setting the delay factor to different values.

23. The arrangement of claim 13 wherein the delay factor of the delay stage is selected to differ from a second delay factor of a second delay stage by an integral multiple.

24. The arrangement of claim 13 wherein m equals n.

25. The arrangement of claim 8 further comprising a microprocessor for processing the input value to generate the decimated sequence of the output value.

26. An arrangement for decimating an input value comprising:

an integrator of an n-th order configured to output the input value to a signal path, the signal path including:

a delay stage configured to adjust the input value that includes a sequence of digital input values using a delay factor, where the delay stage is defined by m times k, m being a positive integer and k being the delay factor;

a decimator configured to convert the input value into a decimated output value using a non-integral factor defined by $M + \alpha$, where M is a positive integer and α is greater than zero and less than one;

a differentiator configured to generate an intermediate output value from the input value; and

an interpolation arrangement configured to receive the intermediate output value and generates a decimated sequence of the output value, wherein the interpolation arrangement interpolates between a plurality of intermediate output values having k/f intervals, wherein f is a sampling rate, the interpolation arrangement including:

a switching device connected to the differentiator, the switching device configured to receive the input value from the differentiator and generate the decimated output value sent to the amplifier arrangement;

an amplifier arrangement connected to the switching device; and

an adder configured to combine the decimated output value of the amplifier arrangement; wherein the amplifier arrangement includes a first amplifier and a second amplifier, the first amplifier having a gain factor of α and the second amplifier having a gain factor of $1 - \alpha$. --

In the abstract:

Replace the abstract with the following version.

-- A comb filter arrangement has an integrator that outputs an input value to a signal path. The signal path includes a delay stage for adjusting the input value using a delay factor, a decimator that converts the input value into a decimated output value using a non-